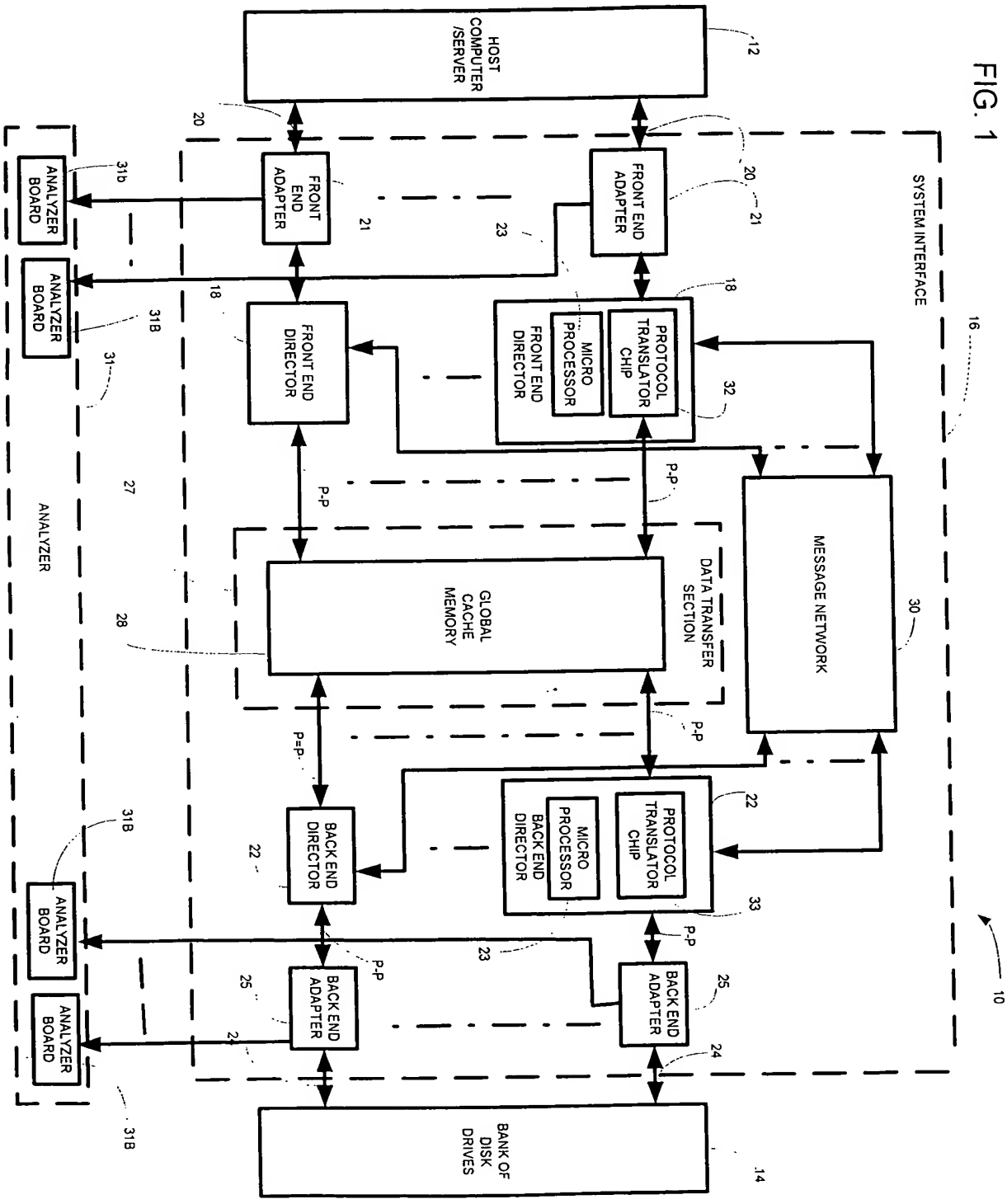
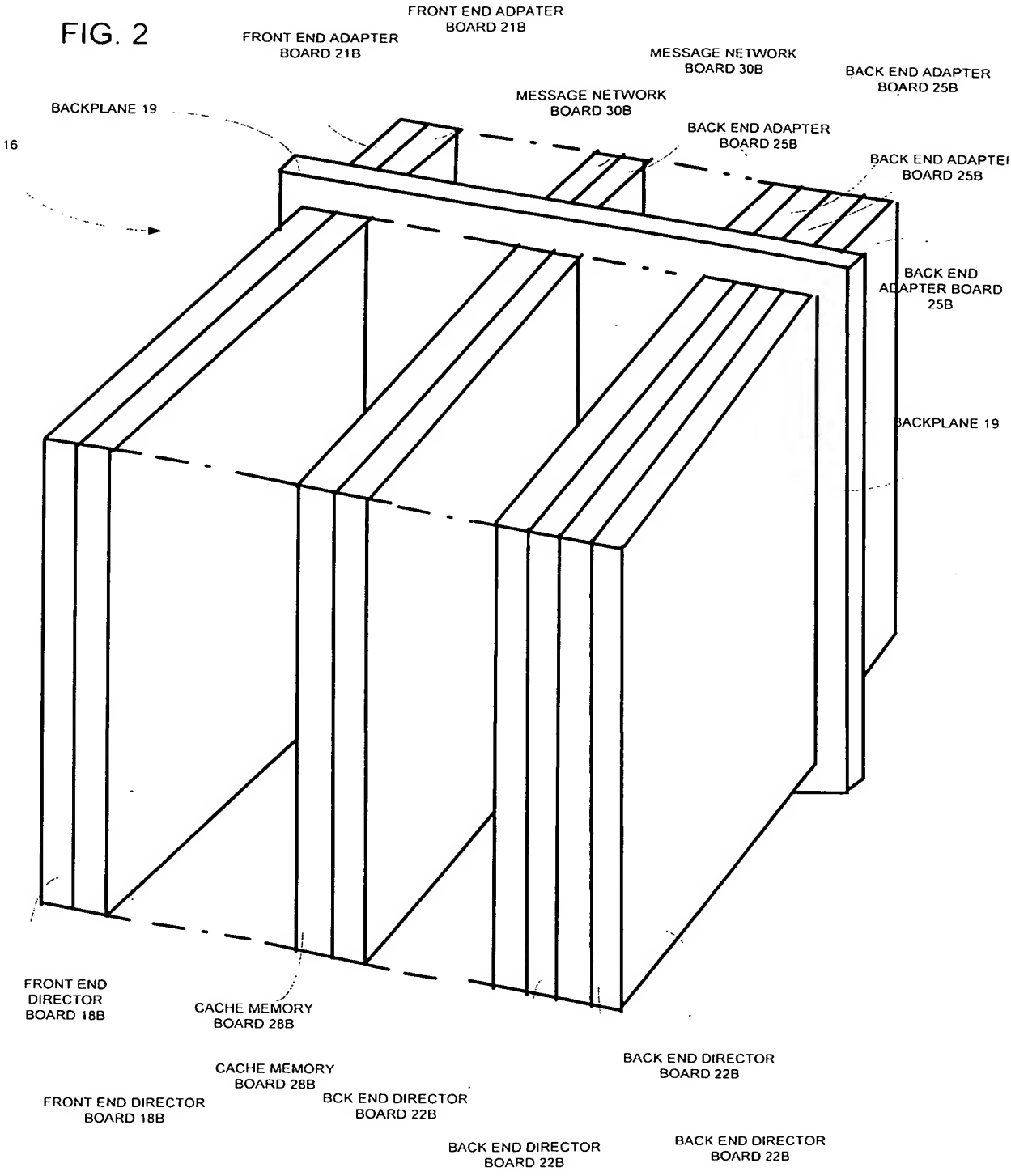

HOST COMPUTER /SERVER
12
20
FRONT END ADAPTER
21
23
FRONT END DIRECTOR
MICRO PROCESSOR
PROTOCOL TRANSLATOR CHIP
18
32
SYSTEM INTERFACE
16
MESSAGE NETWORK
30
P-P
DATA TRANSFER SECTION
GLOBAL CACHE MEMORY
28
27
ANALYZER
ANALYZER BOARD
31b
31B
31
BACK END DIRECTOR
BACK END ADAPTER
22
25
24
33
BANK OF DISK DRIVES
14
10

FIG. 1

FIG. 2


FRONT END ADPATER BOARD 21B
FRONT END ADAPTER BOARD 21B
MESSAGE NETWORK BOARD 30B
BACK END ADAPTER BOARD 25B
MESSAGE NETWORK BOARD 30B
BACKPLANE 19
16
BACK END ADAPTER BOARD 25B
BACK END ADAPTEI BOARD 25B
BACK END ADAPTER BOARD 25B
BACKPLANE 19
FRONT END DIRECTOR BOARD 18B
CACHE MEMORY BOARD 28B
CACHE MEMORY BOARD 28B
BACK END DIRECTOR BOARD 22B
FRONT END DIRECTOR BOARD 18B
BCK END DIRECTOR BOARD 22B
BACK END DIRECTOR BOARD 22B
BACK END DIRECTOR BOARD 22B

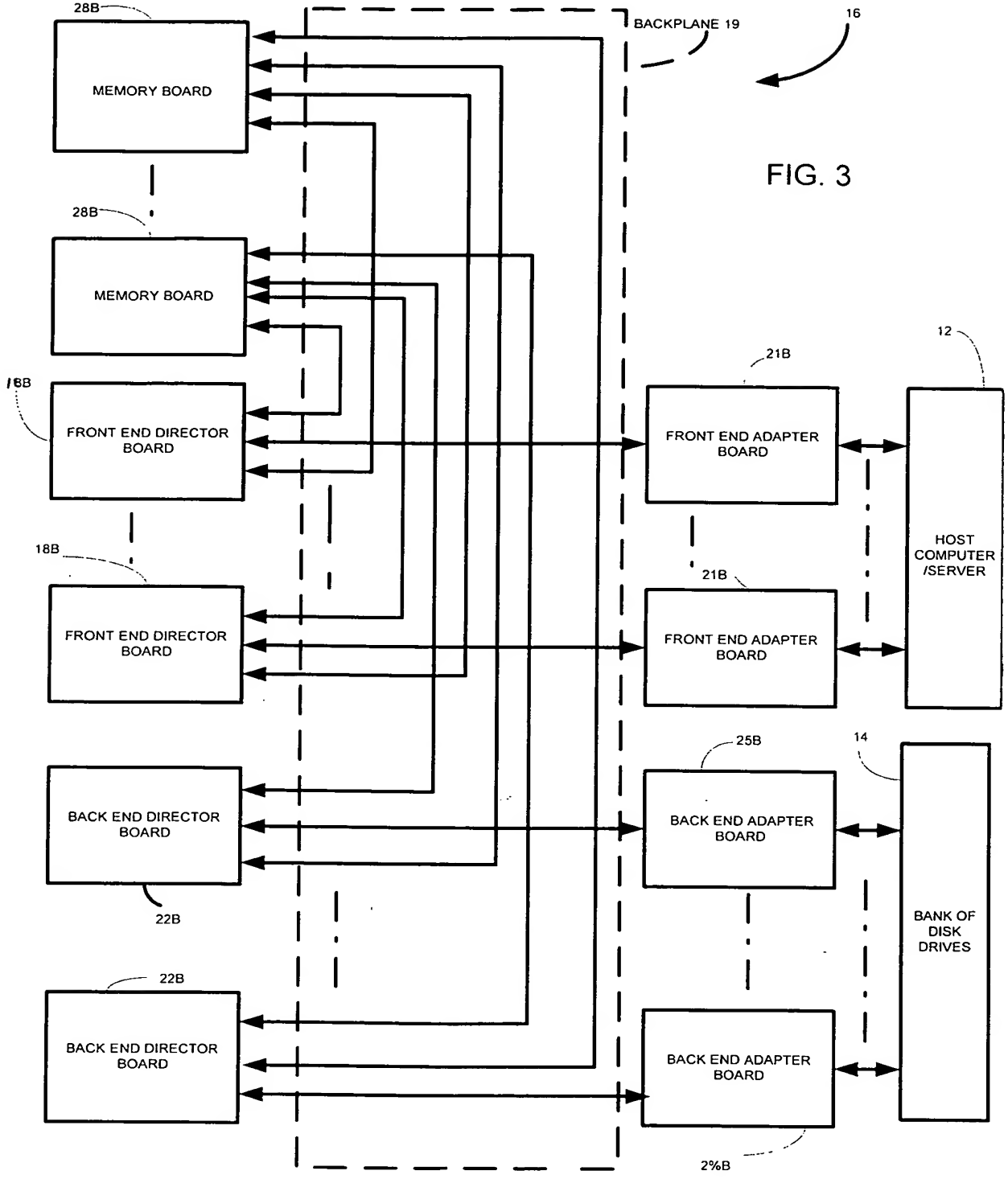

28B
MEMORY BOARD
BACKPLANE 19
16
28B
MEMORY BOARD
12
21B
18B
FRONT END DIRECTOR BOARD
FRONT END ADAPTER BOARD
HOST COMPUTER /SERVER
18B
21B
FRONT END DIRECTOR BOARD
FRONT END ADAPTER BOARD
25B
14
BACK END DIRECTOR BOARD
BACK END ADAPTER BOARD
22B
BANK OF DISK DRIVES
22B
BACK END DIRECTOR BOARD
BACK END ADAPTER BOARD
2%B

FIG. 3

FIG. 4

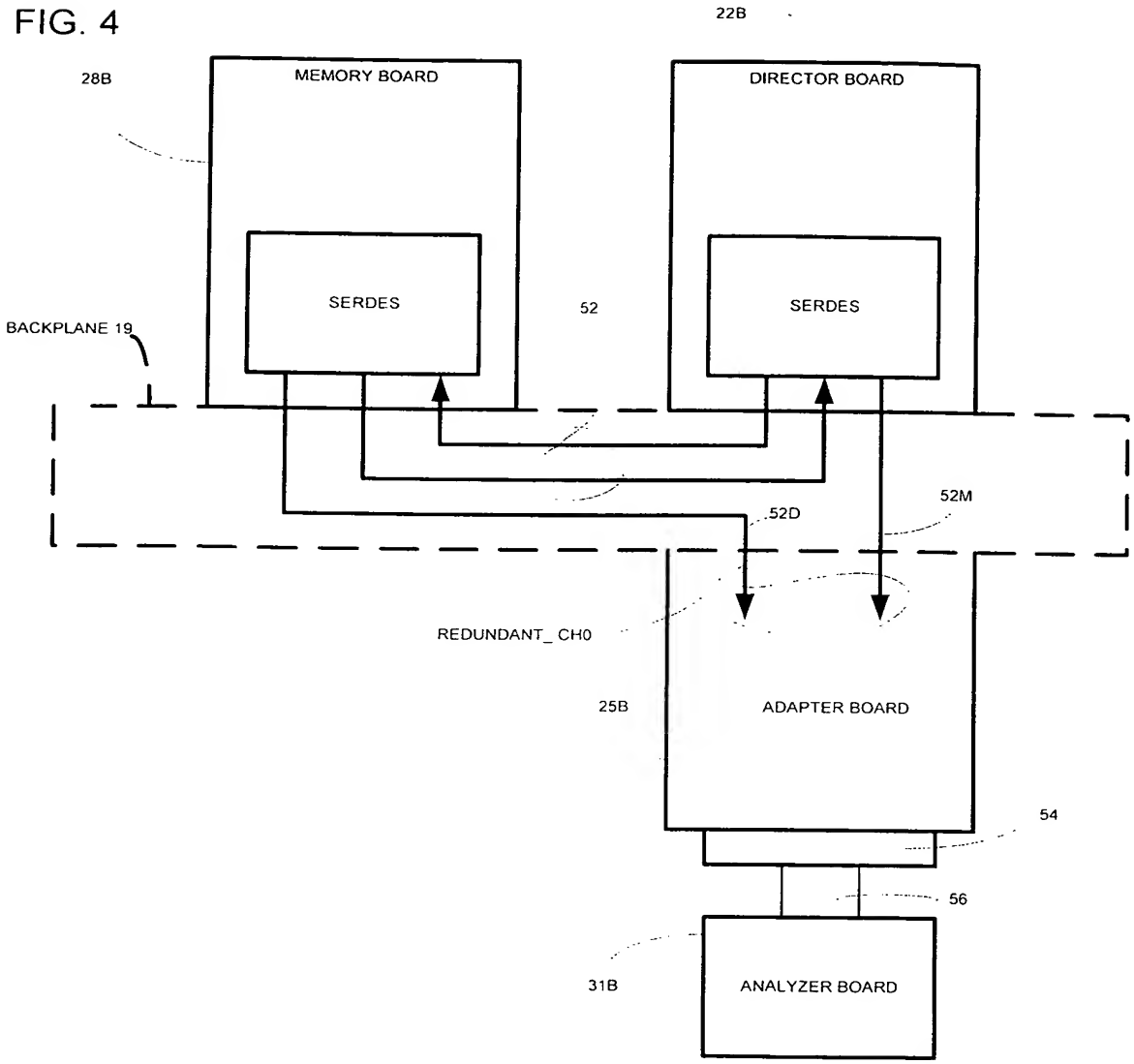

22B
28B
MEMORY BOARD
DIRECTOR BOARD
SERDES
52
SERDES
BACKPLANE 19
52M
52D
REDUNDANT_ CH0
25B
ADAPTER BOARD
54
56
31B
ANALYZER BOARD

FIG. 5

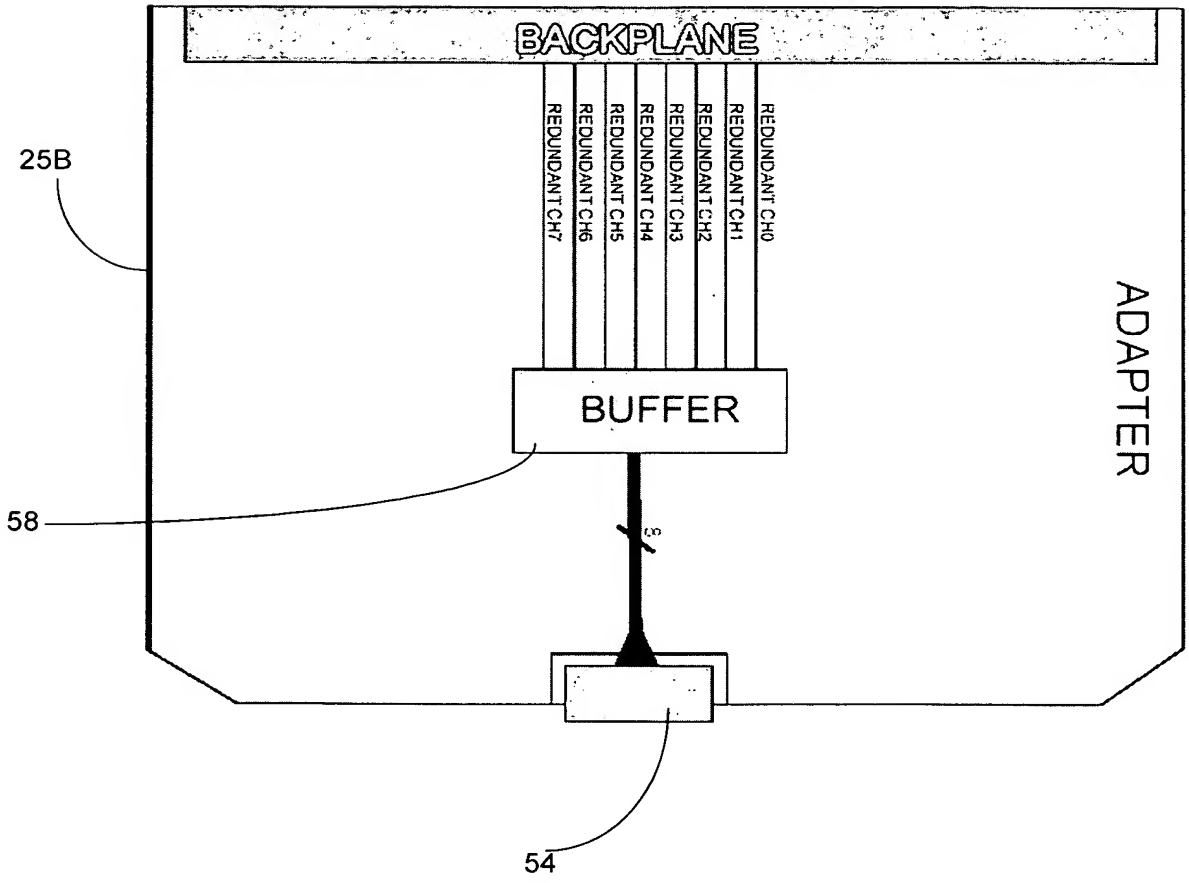
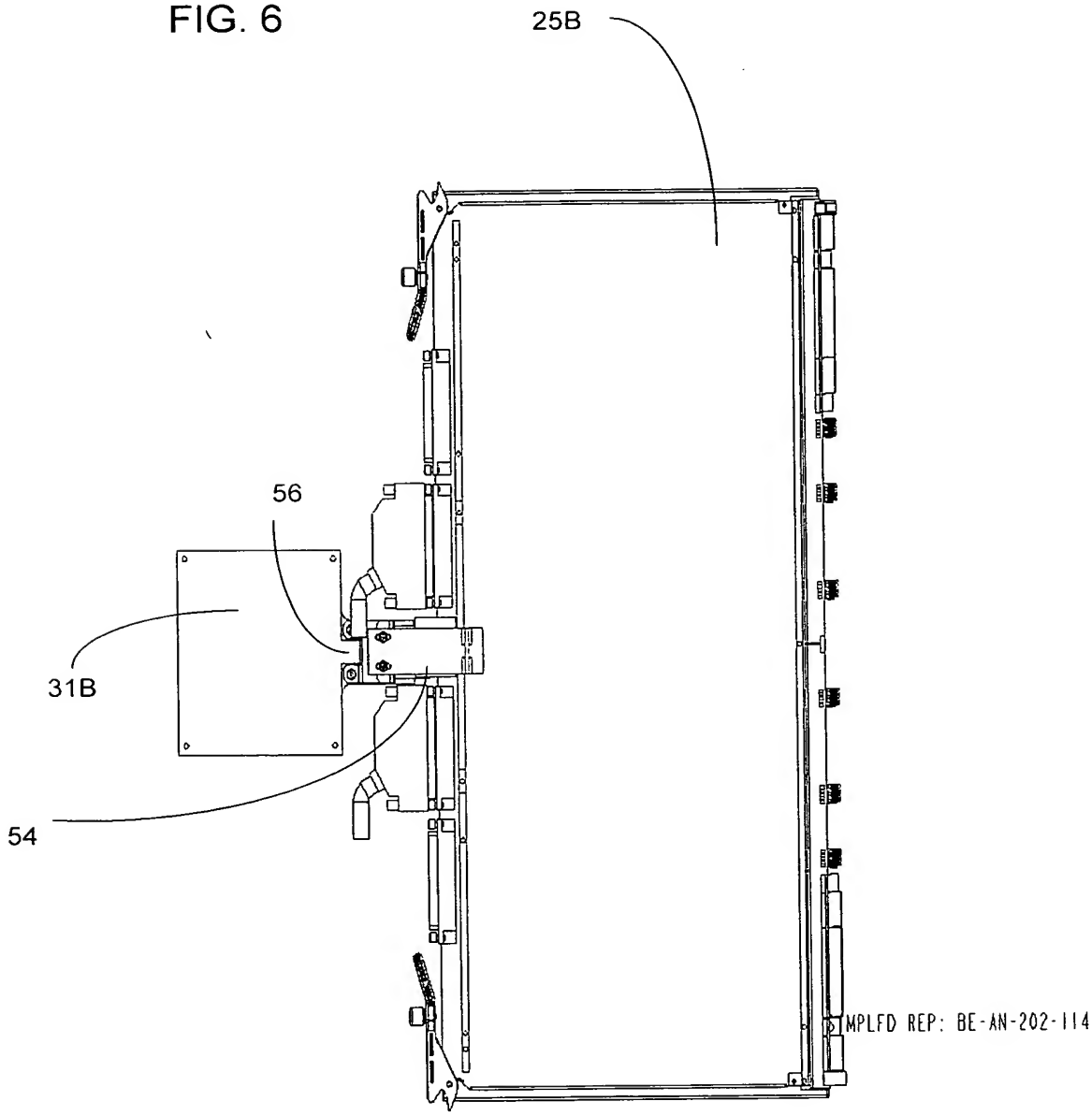

BACKPLANE
REDUNDANT CH7
REDUNDANT CH6
REDUNDANT CH5
REDUNDANT CH4
REDUNDANT CH3
REDUNDANT CH2
REDUNDANT CH1
REDUNDANT CH0
25B
BUFFER
ADAPTER
58
8
54

FIG. 6



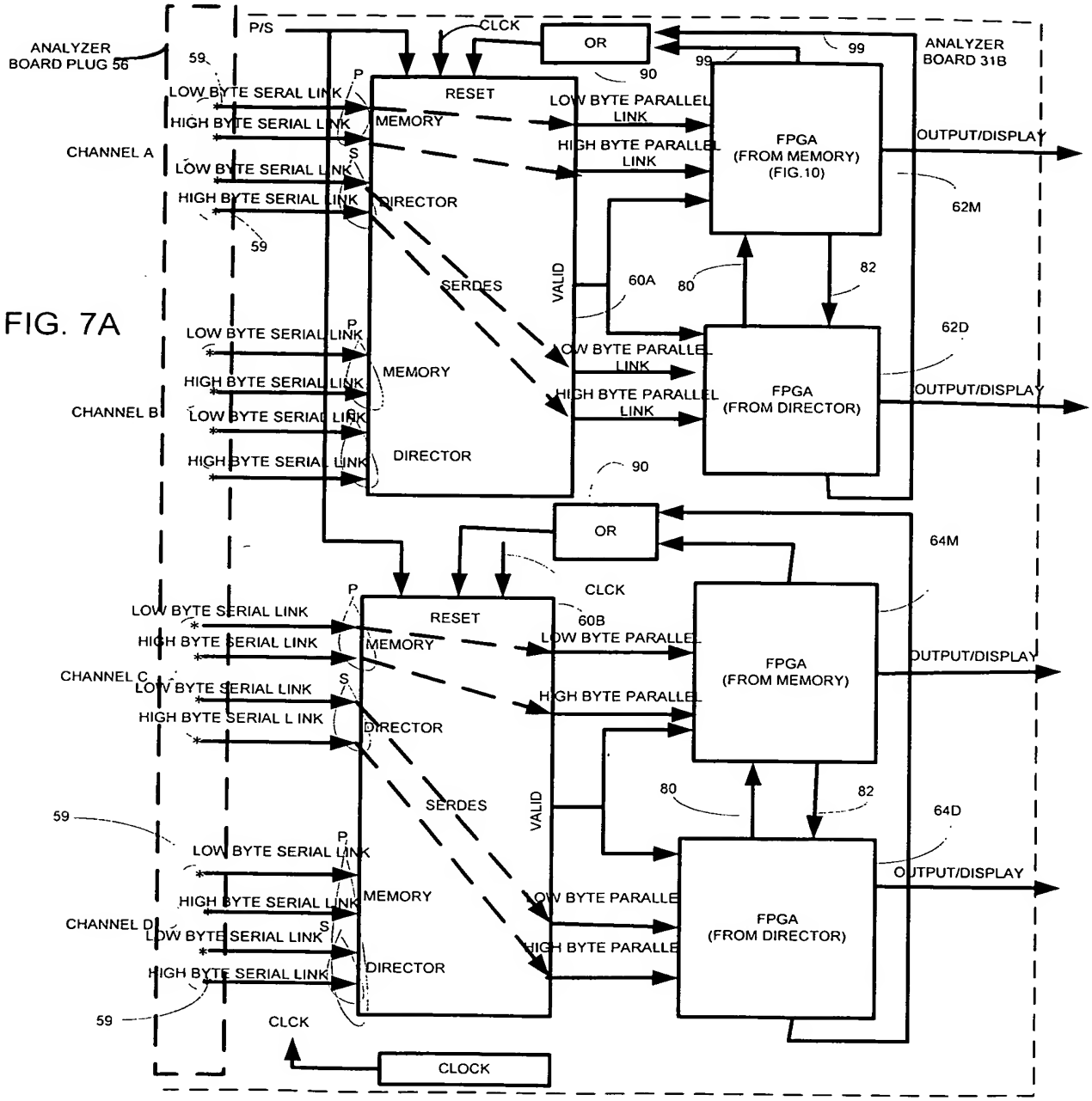
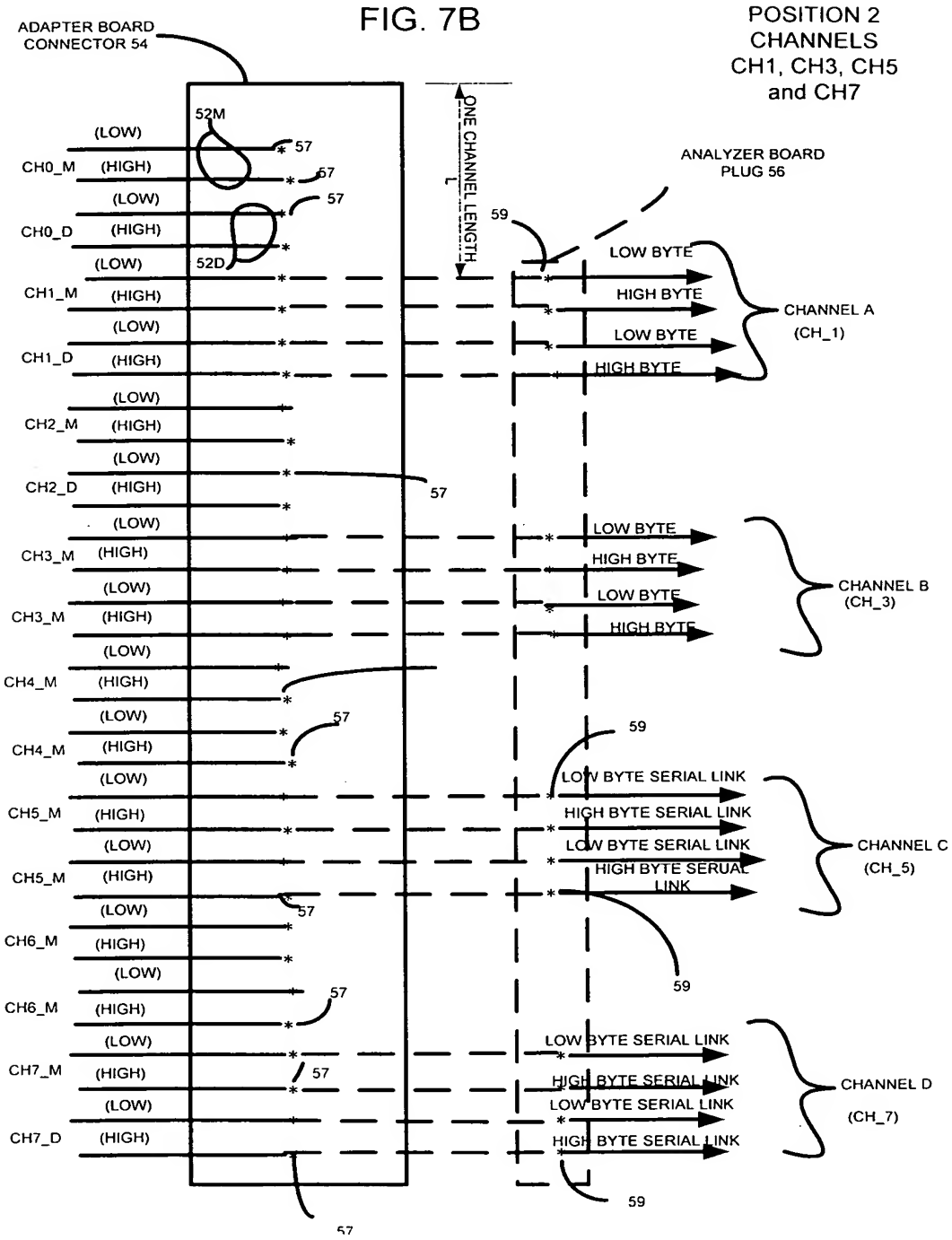

ANALYZER BOARD PLUG 56
59
P/S
CLCK
OR
99
ANALYZER BOARD 31B
90
CHANNEL A
LOW BYTE SERAL LINK
HIGH BYTE SERIAL LINK
LOW BYTE SERIAL LINK
HIGH BYTE SERIAL LINK
P
S
RESET
MEMORY
DIRECTOR
SERDES
VALID
LOW BYTE PARALLEL LINK
HIGH BYTE PARALLEL LINK
FPGA (FROM MEMORY) (FIG.10)
OUTPUT/DISPLAY
62M
60A
80
82
62D
FPGA (FROM DIRECTOR)
CHANNEL B
64M
CLCK
60B
CHANNEL C
FPGA (FROM MEMORY)
64D
CHANNEL D
FPGA (FROM DIRECTOR)
CLOCK

FIG. 7A

FIG. 7B


POSITION 2
CHANNELS
CH1, CH3, CH5
and CH7
ADAPTER BOARD
CONNECTOR 54
ANALYZER BOARD
PLUG 56
ONE CHANNEL LENGTH
52M
52D
59
57
(LOW)
(HIGH)
CH0_M
CH0_D
CH1_M
CH1_D
CH2_M
CH2_D
CH3_M
CH4_M
CH5_M
CH6_M
CH7_M
CH7_D
LOW BYTE
HIGH BYTE
CHANNEL A
(CH_1)
CHANNEL B
(CH_3)
LOW BYTE SERIAL LINK
HIGH BYTE SERIAL LINK
CHANNEL C
(CH_5)
CHANNEL D
(CH_7)

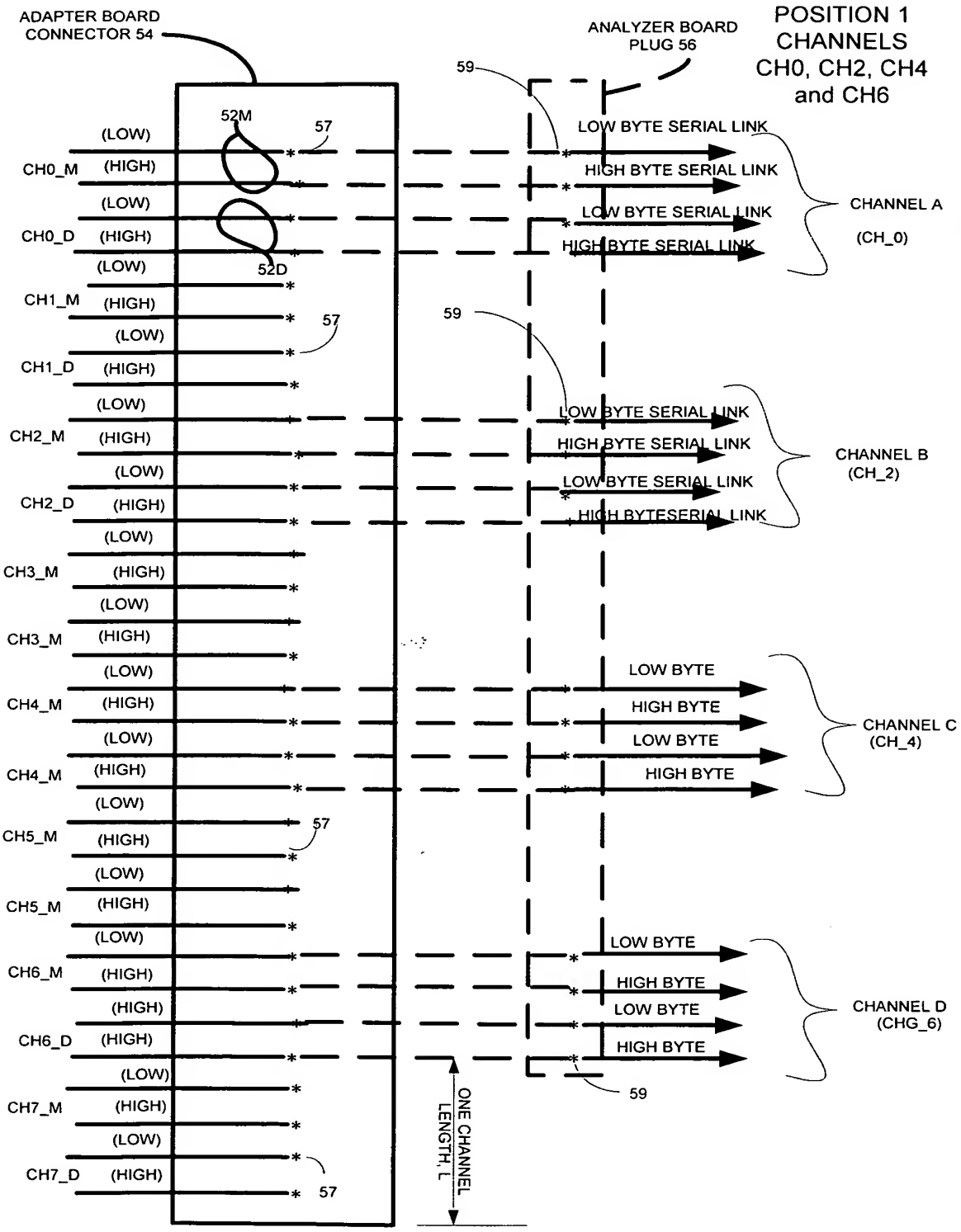
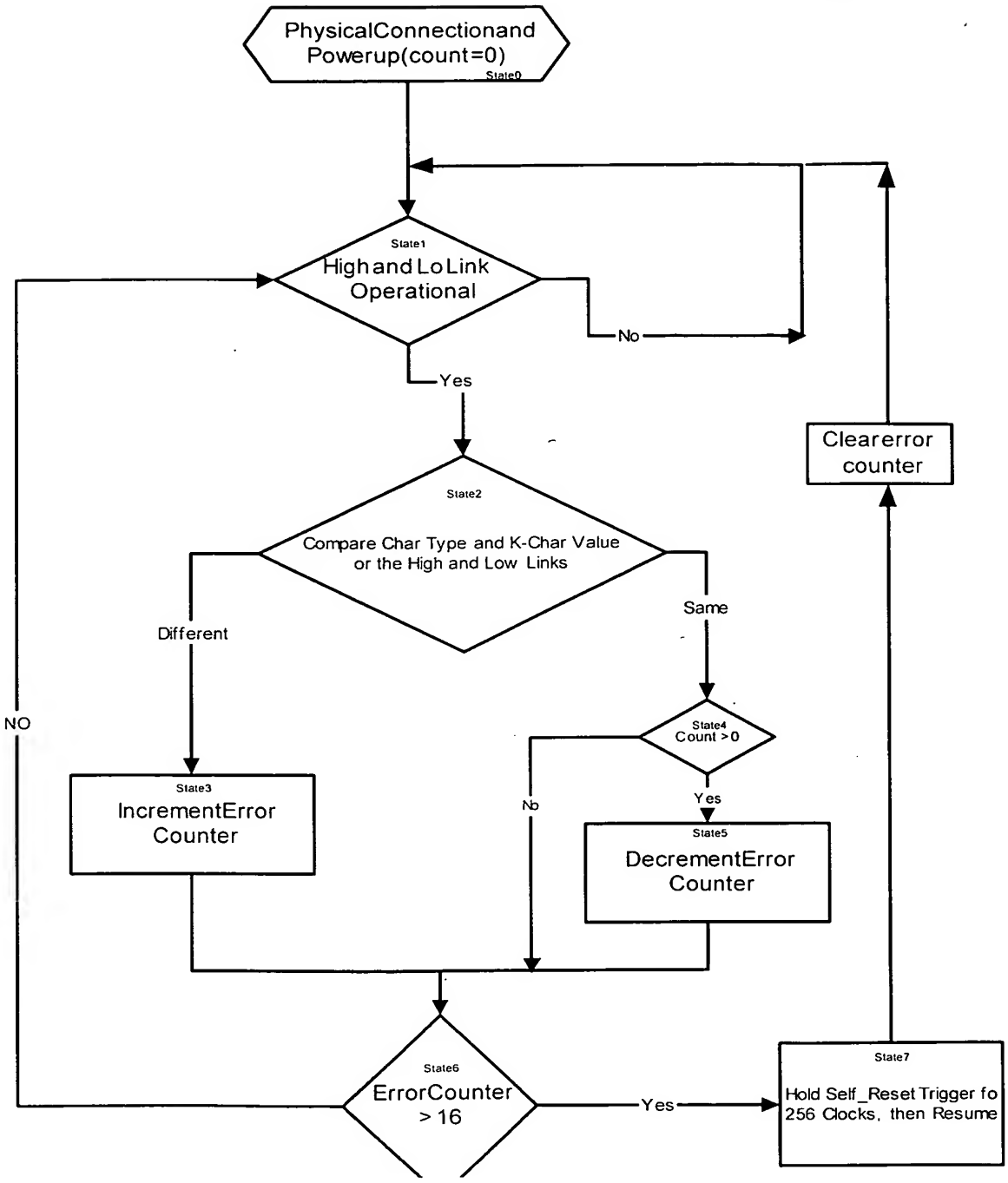

ADAPTER BOARD CONNECTOR 54
ANALYZER BOARD PLUG 56
POSITION 1 CHANNELS CH0, CH2, CH4 and CH6
52M
52D
57
59
(LOW)
(HIGH)
CH0_M
CH0_D
CH1_M
CH1_D
CH2_M
CH2_D
CH3_M
CH4_M
CH5_M
CH6_M
CH6_D
CH7_M
CH7_D
LOW BYTE SERIAL LINK
HIGH BYTE SERIAL LINK
CHANNEL A (CH_0)
CHANNEL B (CH_2)
LOW BYTE
HIGH BYTE
CHANNEL C (CH_4)
CHANNEL D (CHG_6)
ONE CHANNEL LENGTH, L

FIG. 7C

FIG. 8


PhysicalConnectionand Powerup(count=0)
State0
State1
High and Lo Link Operational
No
Yes
State2
Compare Char Type and K-Char Value or the High and Low Links
Different
Same
NO
State3
IncrementError Counter
State4
Count >0
No
Yes
State5
DecrementError Counter
State6
ErrorCounter > 16
Yes
State7
Hold Self_Reset Trigger fo 256 Clocks, then Resume
Clearerror counter

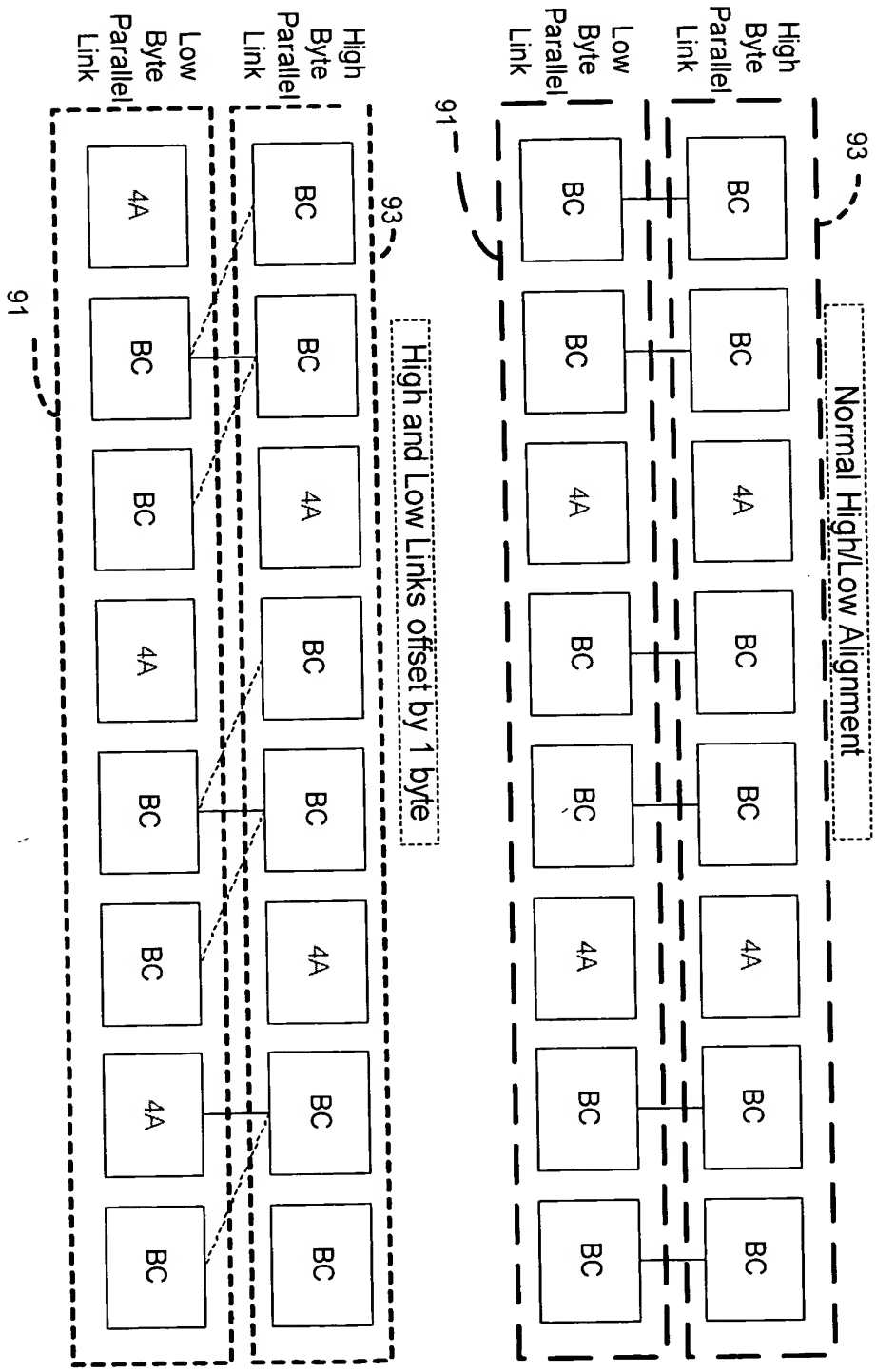

Normal High/Low Alignment
High Byte Parallel Link
Low Byte Parallel Link
93
91
BC
4A
High and Low Links offset by 1 byte

FIG. 9

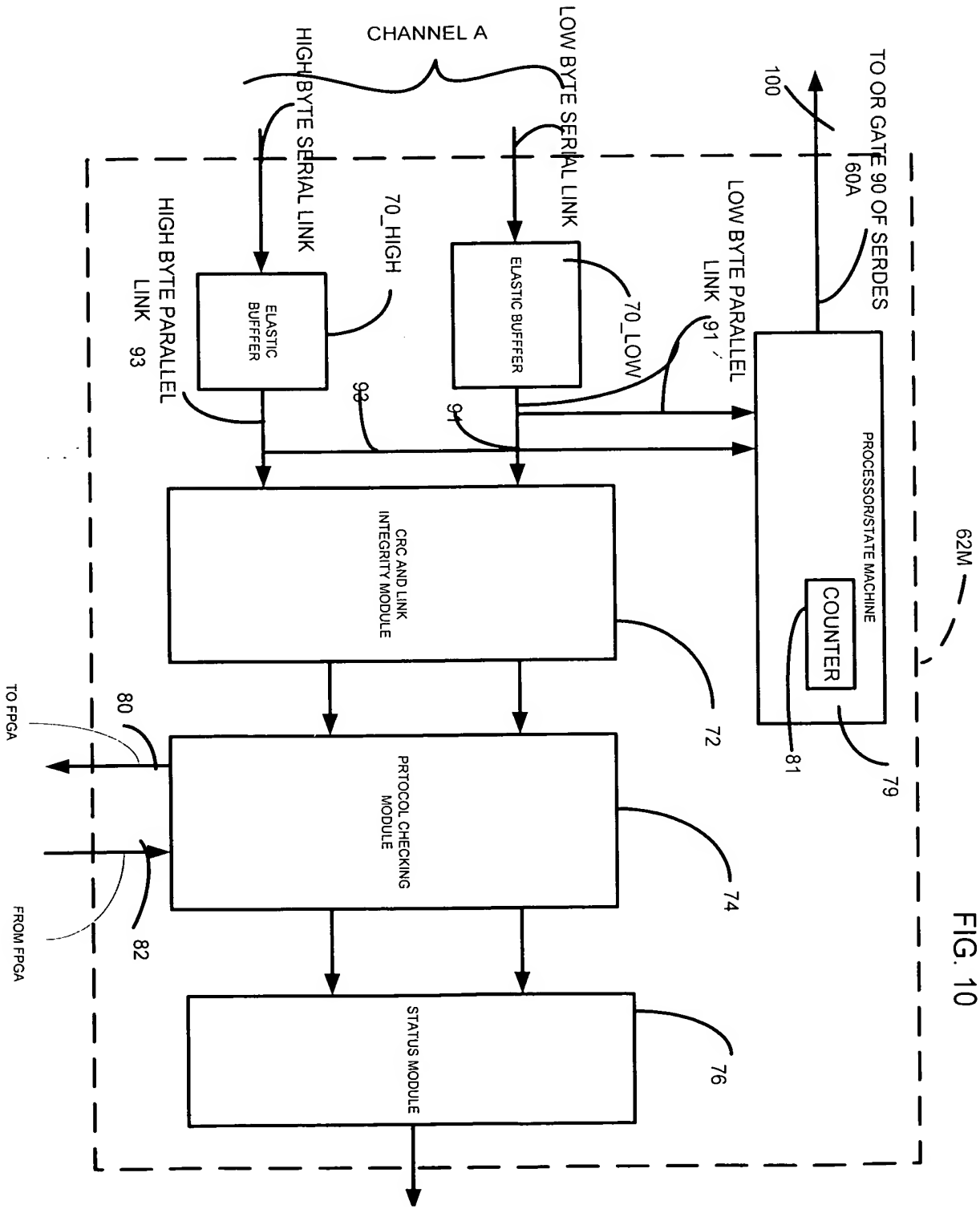

CHANNEL A
HIGH BYTE SERIAL LINK
LOW BYTE SERIAL LINK
TO OR GATE 90 OF SERDES
60A
100
70_HIGH
70_LOW
ELASTIC BUFFFER
ELASTIC BUFFFER
HIGH BYTE PARALLEL LINK 93
LOW BYTE PARALLEL LINK 91
98
94
PROCESSOR/STATE MACHINE
COUNTER
62M
CRC AND LINK INTEGRITY MODULE
72
80
TO FPGA
PRTOCOL CHECKING MODULE
74
FROM FPGA
82
81
79
STATUS MODULE
76

FIG. 10